METHOD OF POWER DISTRIBUTION ANALYSIS FOR I/O CIRCUITS IN ASIC DESIGNS

ABSTRACT OF THE DISCLOSURE

A method and system for testing the compliance of a distribution of I/O circuits in a semiconductor chip with voltage (IR) and electromigration (EM) limits. Maximum and average currents for the I/O circuits are calculated. A resistance model for the power distribution network of the chip is created, and the I/O circuit currents are indexed to corresponding nodes in the resistance model. Average current demand of the logic circuitry of the chip is also calculated and indexed to nodes in the resistance model. The resistance model with indexed currents is then solved to determine voltages at the nodes. The voltages are checked for compliance with IR and EM limits, and a report is produced. If violations of the IR and EM limits are detected, the placement of the I/O circuits in the power distribution network may be revised to bring the design into compliance with IR and EM requirements.